# Features

- **High Performance, Low Power AVR® 8-bit Microcontroller**
- **Advanced RISC Architecture**
    - **124 Powerful Instructions - Most Single Clock Cycle Execution**
    - **32 x 8 General Purpose Working Registers**
    - **Fully Static Operation**
    - **Up to 1 MIPS Throughput at 1 MHz**
- **Nonvolatile Program and Data Memories**
    - **40K Bytes of In-System Self-Programmable Flash, Endurance: 10,000 Write/Erase Cycles**
    - **Optional Boot Code Section with Independent Lock Bits**
      **In-System Programming by On-chip Boot Program**
      **True Read-While-Write Operation**
    - **512 bytes EEPROM, Endurance: 100,000 Write/Erase Cycles**
    - **2K Bytes Internal SRAM**
    - **Programming Lock for Software Security**
- **On-chip Debugging**
    - **Extensive On-chip Debug Support**
    - **Available through JTAG interface**
- **Battery Management Features**
    - **Two, Three, or Four Cells in Series**
    - **Deep Under-voltage Protection**
    - **Over-current Protection (Charge and Discharge)**
    - **Short-circuit Protection (Discharge)**
    - **Integrated Cell Balancing FETs**
    - **High Voltage Outputs to Drive Charge/Precharge/Discharge FETs**
- **Peripheral Features**
    - **One 8-bit Timer/Counter with Separate Prescaler, Compare Mode, and PWM**
    - **One 16-bit Timer/Counter with Separate Prescaler and Compare Mode**
    - **12-bit Voltage ADC, Eight External and Two Internal ADC Inputs**
    - **High Resolution Coulomb Counter ADC for Current Measurements**
    - **TWI Serial Interface for SM-Bus**
    - **Programmable Wake-up Timer**
    - **Programmable Watchdog Timer**
- **Special Microcontroller Features**
    - **Power-on Reset**
    - **On-chip Voltage Regulator**
    - **External and Internal Interrupt Sources**
    - **Four Sleep Modes: Idle, Power-save, Power-down, and Power-off**
- **Packages**
    - **48-pin LQFP**
- **Operating Voltage: 4.0 - 25V**
- **Maximum Withstand Voltage (High-voltage pins): 28V**
- **Temperature Range: -30°C to 85°C**
    - **Speed Grade: 1 MHz**

**8-bit AVR® Microcontroller with 40K Bytes In-System Programmable Flash**
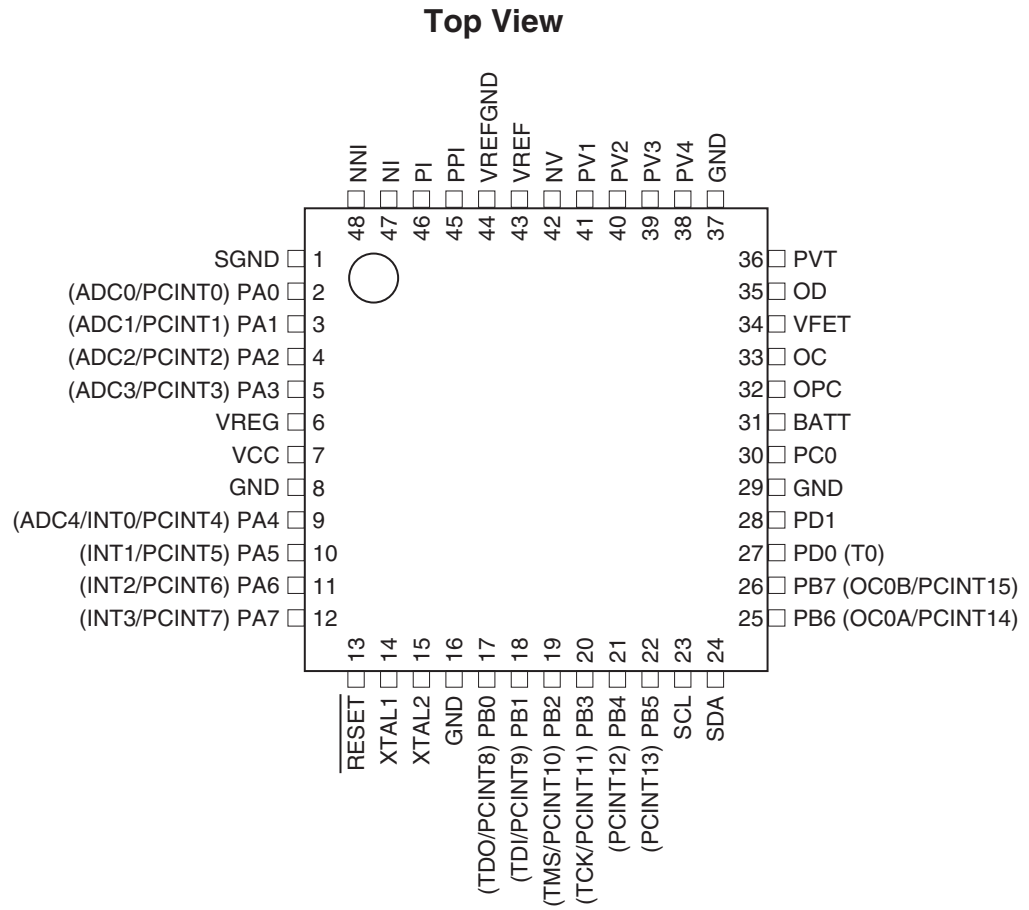
**ATmega406**

**Preliminary Summary**

Note: This is a summary document. A complete document is available on our Web site at www.atmel.com.

# 1. Pin Configurations

**Figure 1-1.** Pinout ATmega406.

**Top View**



## 1.1 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## 2. Overview

The ATmega406 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega406 achieves throughputs approaching 1 MIPS at 1 MHz.

### 2.1 Block Diagram

**Figure 2-1.** Block Diagram
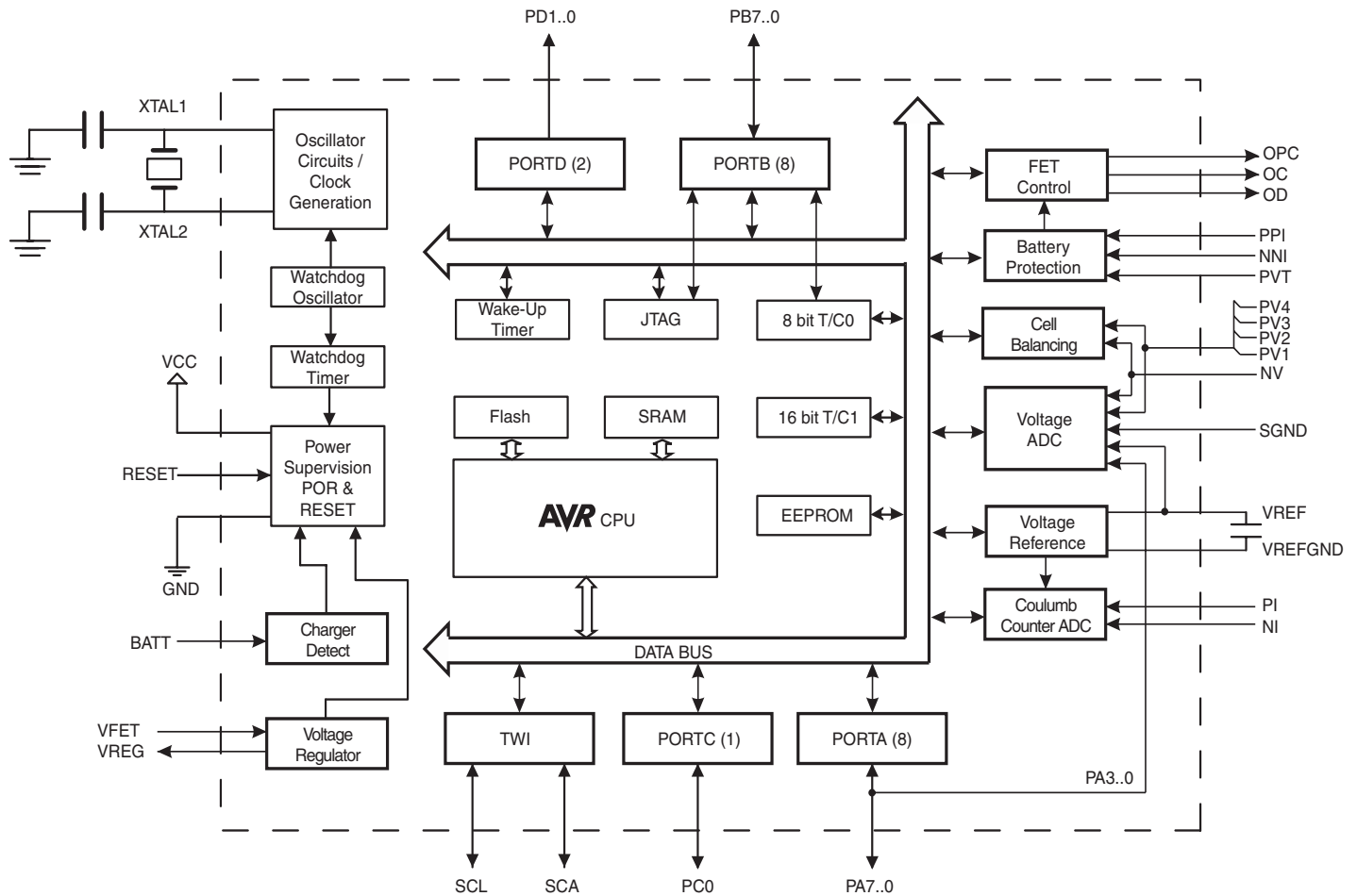


The ATmega406 provides the following features: a Voltage Regulator, dedicated Battery Protection Circuitry, integrated cell balancing FETs, high-voltage analog front-end, and an MCU with two ADCs with On-chip voltage reference for battery fuel gauging.

The voltage regulator operates at a wide range of voltages, 4.0 - 25 volts. This voltage is regulated to a constant supply voltage of nominally 3.3 volts for the integrated logic and analog functions.

The battery protection monitors the battery voltage and charge/discharge current to detect illegal conditions and protect the battery from these when required. The illegal conditions are deep under-voltage during discharging and short-circuit during discharging, and over-current during charging and discharging.

The integrated cell balancing FETs allow cell balancing algorithms to be implemented in software.

The MCU provides the following features: 40K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512 bytes EEPROM, 2K byte SRAM, 32 general purpose working registers, 18 general purpose I/O lines, 11 high-voltage I/O lines, a JTAG Interface for On-chip Debugging support and programming, two flexible Timer/Counters with PWM and compare modes, one Wake-up Timer, an SM-Bus compliant TWI module, internal and external interrupts, a 12-bit Sigma Delta ADC for voltage and temperature measurements, a high resolution Sigma Delta ADC for Coulomb Counting and instantaneous current measurements, a programmable Watchdog Timer with internal Oscillator, and four software selectable power saving modes.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Idle mode stops the CPU while allowing the other chip function to continue functioning. The Power-down mode allows the voltage regulator, battery protection, regulator current detection, Watchdog Timer, and Wake-up Timer to operate, while disabling all other chip functions until the next Interrupt or Hardware Reset. In Power-save mode, the Wake-up Timer and Coulomb Counter ADC continues to run.

The device is manufactured using Atmel's high voltage high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System, by a conventional non-volatile memory programmer or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash, fuel gauging ADCs, dedicated battery protection circuitry, Cell Balancing FETs, and a voltage regulator on a monolithic chip, the Atmel ATmega406 is a powerful microcontroller that provides a highly flexible and cost effective solution for Li-ion Smart Battery applications.

The ATmega406 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and On-chip Debugger.

## 2.2    Pin Descriptions

### 2.2.1    VFET

Input to the internal voltage regulator.

### 2.2.2    VCC

Digital supply voltage. Normally connected to VREG.

### 2.2.3    VREG

Output from the internal voltage regulator.

### 2.2.4    VREF

Internal Voltage Reference for external decoupling.

### 2.2.5    VREFGND

Ground for decoupling of Internal Voltage Reference.

### 2.2.6    GND

Ground

### 2.2.7    SGND

Signal Ground.

### 2.2.8    Port A (PA7:PA0)

PA3:PA0 serves as the analog inputs to the Voltage A/D Converter.

Port A also serves as a low-voltage 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega406 as listed in "Alternate Functions of Port A" on page 69.

### 2.2.9    Port B (PB7:PB0)

Port B is a low-voltage 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega406 as listed in "Alternate Functions of Port B" on page 71.

### 2.2.10    Port C (PC0)

Port C is a high voltage Open Drain output port.

### 2.2.11    Port D (PD1:PD0)

Port D is a low-voltage 2-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). As inputs, Port D pins that are externally pulled low will source current if the pull-up

resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega406 as listed in "Alternate Functions of Port D" on page 73.

**2.2.12  SCL**

SMBUS clock, Open Drain bidirectional pin.

**2.2.13  SDA**

SMBUS data, Open Drain bidirectional pin.

**2.2.14  OC**

High voltage output to drive Charge FET.

**2.2.15  OD**

High voltage output to drive Discharge FET.

**2.2.16  OPC**

High voltage output to drive Pre-charge FET.

**2.2.17  NI**

NI is the filtered negative input from the current sense resistor.

**2.2.18  NNI**

NNI is the unfiltered negative input from the current sense resistor.

**2.2.19  PI**

PI is the filtered positive input from the current sense resistor.

**2.2.20  PPI**

PPI is the unfiltered positive input from the current sense resistor.

**2.2.21  NV/PV1/PV2/PV3/PV4**

NV, PV1, PV2, PV3, and PV4 are the inputs for battery cells 1, 2, 3, and 4.

**2.2.22  PVT**

PVT is the sense input for deep under-voltage protection. This pin also defines the pull-up level for the OD output.

**2.2.23  BATT**

Input for detecting when a charger is connected. This pin also defines the pull-up level for OC and OPC outputs.

**2.2.24  RESET**

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 11 on page 38. Shorter pulses are not guaranteed to generate a reset.

**2.2.25    XTAL1**

Input to the inverting Oscillator amplifier.

**2.2.26    XTAL2**

Output from the inverting Oscillator amplifier.

# 3.    About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

## 4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| (0xFF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xFA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xF8) | BPPLR | – | – | – | – | – | – | BPPLE | BPPL | 158 |
| (0xF7) | BPCR | – | – | – | – | DUVD | SCD | DCD | CCD | 158 |
| (0xF6) | CBPTR | | | SCPT[3:0] | | | | OCPT[3:0] | | 159 |
| (0xF5) | BPOCD | | | DCDL[3:0] | | | | CCDL[3:0] | | 159 |
| (0xF4) | BPSCD | – | – | – | – | | | SCDL[3:0] | | 160 |
| (0xF3) | BPDUV | – | – | DUVT1 | DUVT0 | | | DUDL[3:0] | | 161 |
| (0xF2) | BPIR | DUVIF | COCIF | DOCIF | SCIF | DUVIE | COCIE | DOCIE | SCIE | 161 |
| (0xF1) | CBCR | – | – | – | CBE4 | CBE3 | CBE2 | CBE1 | | 168 |
| (0xF0) | FCSR | – | – | PWMOC | PWMOPC | CPS | DFE | CFE | PFD | 164 |
| (0xEF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xED) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xEA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xE9) | CADICH | | | | | CADIC[15:8] | | | | 143 |
| (0xE8) | CADICL | | | | | CADIC[7:0] | | | | 143 |
| (0xE7) | CADRDC | | | | | CADRDC[7:0] | | | | 144 |
| (0xE6) | CADRCC | | | | | CADRCC[7:0] | | | | 143 |
| (0xE5) | CADCSRB | – | CADACIE | CADRCIE | CADICIE | – | CADACIF | CADRCIF | CADICIF | 142 |
| (0xE4) | CADCSRA | CADEN | – | CADUB | CADAS1 | CADAS0 | CADSI1 | CADSI0 | CADSE | 140 |
| (0xE3) | CADAC3 | | | | | CADAC[31:24] | | | | 143 |
| (0xE2) | CADAC2 | | | | | CADAC[23:16] | | | | 143 |
| (0xE1) | CADAC1 | | | | | CADAC[15:8] | | | | 143 |
| (0xE0) | CADAC0 | | | | | CADAC[7:0] | | | | 143 |
| (0xDF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xDA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xD1) | BGCRR | BGCR7 | BGCR6 | BGCR5 | BGCR4 | BGCR3 | BGCR2 | BGCR1 | BGCR0 | 152 |
| (0xD0) | BGCCR | BGEN | – | BGCC5 | BGCC4 | BGCC3 | BGCC2 | BGCC1 | BGCC0 | 152 |
| (0xCF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xCA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xC0) | CCSR | – | – | – | – | – | – | XOE | ACS | 31 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---------|------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| (0xBF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xBE) | TWBCSR | TWBCIF | TWBCIE | – | – | – | TWBDT1 | TWBDT0 | TWBCIP | 137 |
| (0xBD) | TWAMR | TWAM[6:0] | | | | | | | – | 118 |
| (0xBC) | TWCR | TWINT | TWEA | TWSTA | TWSTO | TWWC | TWEN | – | TWIE | 115 |
| (0xBB) | TWDR | 2–wire Serial Interface Data Register | | | | | | | | 117 |
| (0xBA) | TWAR | TWA[6:0] | | | | | | | TWGCE | 117 |
| (0xB9) | TWSR | TWS[7:3] | | | | | – | TWPS1 | TWPS0 | 116 |
| (0xB8) | TWBR | 2–wire Serial Interface Bit Rate Register | | | | | | | | 115 |
| (0xB7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xB0) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAF) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAE) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAD) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAC) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAB) | Reserved | – | – | – | – | – | – | – | – | |
| (0xAA) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA9) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA8) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA7) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA6) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA5) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA4) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA3) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA2) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA1) | Reserved | – | – | – | – | – | – | – | – | |
| (0xA0) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9B) | Reserved | – | – | – | – | – | – | – | – | |
| (0x9A) | Reserved | – | – | – | – | – | – | – | – | |
| (0x99) | Reserved | – | – | – | – | – | – | – | – | |
| (0x98) | Reserved | – | – | – | – | – | – | – | – | |
| (0x97) | Reserved | – | – | – | – | – | – | – | – | |
| (0x96) | Reserved | – | – | – | – | – | – | – | – | |
| (0x95) | Reserved | – | – | – | – | – | – | – | – | |
| (0x94) | Reserved | – | – | – | – | – | – | – | – | |
| (0x93) | Reserved | – | – | – | – | – | – | – | – | |
| (0x92) | Reserved | – | – | – | – | – | – | – | – | |
| (0x91) | Reserved | – | – | – | – | – | – | – | – | |
| (0x90) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8E) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8C) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8B) | Reserved | – | – | – | – | – | – | – | – | |
| (0x8A) | Reserved | – | – | – | – | – | – | – | – | |
| (0x89) | OCR1AH | Timer/Counter1 – Output Compare Register A High Byte | | | | | | | | 103 |
| (0x88) | OCR1AL | Timer/Counter1 – Output Compare Register A Low Byte | | | | | | | | 103 |
| (0x87) | Reserved | – | – | – | – | – | – | – | – | |
| (0x86) | Reserved | – | – | – | – | – | – | – | – | |
| (0x85) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | 103 |
| (0x84) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | 103 |
| (0x83) | Reserved | – | – | – | – | – | – | – | – | |
| (0x82) | Reserved | – | – | – | – | – | – | – | – | |
| (0x81) | TCCR1B | – | – | – | – | CTC1 | CS12 | CS11 | CS10 | 102 |
| (0x80) | Reserved | – | – | – | – | – | – | – | – | |
| (0x7F) | Reserved | – | – | – | – | – | – | – | – | |
| (0x7E) | DIDR0 | – | – | – | – | VADC3D | VADC2D | VADC1D | VADC0D | 150 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| (0x7D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x7C) | VADMUX | – | – | – | – | VADMUX3 | VADMUX2 | VADMUX1 | VADMUX0 | 148 |
| (0x7B) | Reserved | – | – | – | – | – | – | – | – | |
| (0x7A) | VADCSR | – | – | – | – | VADEN | VADSC | VADCCIF | VADCCIE | 149 |
| (0x79) | VADCH | – | – | – | | VADC Data Register High byte | | | | 149 |
| (0x78) | VADCL | | | | VADC Data Register Low byte | | | | | 149 |
| (0x77) | Reserved | – | – | – | – | – | – | – | – | |
| (0x76) | Reserved | – | – | – | – | – | – | – | – | |
| (0x75) | Reserved | – | – | – | – | – | – | – | – | |
| (0x74) | Reserved | – | – | – | – | – | – | – | – | |
| (0x73) | Reserved | – | – | – | – | – | – | – | – | |
| (0x72) | Reserved | – | – | – | – | – | – | – | – | |
| (0x71) | Reserved | – | – | – | – | – | – | – | – | |
| (0x70) | Reserved | – | – | – | – | – | – | – | – | |
| (0x6F) | TIMSK1 | – | – | – | – | – | – | OCIE1A | TOIE1 | 104 |
| (0x6E) | TIMSK0 | – | – | – | – | – | OCIE0B | OCIE0A | TOIE0 | 95 |
| (0x6D) | Reserved | – | – | – | – | – | – | – | – | |
| (0x6C) | PCMSK1 | | | | PCINT[15:8] | | | | | 60 |
| (0x6B) | PCMSK0 | | | | PCINT[7:0] | | | | | 60 |
| (0x6A) | Reserved | – | – | – | – | – | – | – | | |
| (0x69) | EICRA | ISC31 | ISC30 | ISC21 | ISC20 | ISC11 | ISC10 | ISC01 | ISC00 | 57 |
| (0x68) | PCICR | – | – | – | – | – | – | PCIE1 | PCIE0 | 59 |
| (0x67) | Reserved | – | – | – | – | – | – | – | – | |
| (0x66) | FOSCCAL | | | | Fast Oscillator Calibration Register | | | | | 29 |
| (0x65) | Reserved | – | – | – | – | – | – | – | – | |
| (0x64) | PRR0 | – | – | – | – | PRTWI | PRTIM1 | PRTIM0 | PRVADC | 37 |
| (0x63) | Reserved | – | – | – | – | – | – | – | – | |
| (0x62) | WUTCSR | WUTIF | WUTIE | WUTCF | WUTR | WUTE | WUTP2 | WUTP1 | WUTP0 | 49 |
| (0x61) | Reserved | – | – | – | – | – | – | – | – | |
| (0x60) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | 47 |
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 11 |
| 0x3E (0x5E) | SPH | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 | 13 |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 13 |
| 0x3C (0x5C) | Reserved | – | – | – | – | – | – | – | – | |
| 0x3B (0x5B) | Reserved | – | – | – | – | – | – | – | – | |
| 0x3A (0x5A) | Reserved | – | – | – | – | – | – | – | – | |
| 0x39 (0x59) | Reserved | – | – | – | – | – | – | – | – | |
| 0x38 (0x58) | Reserved | – | – | – | – | – | – | – | – | |
| 0x37 (0x57) | SPMCSR | SPMIE | RWWSB | SIGRD | RWWSRE | BLBSET | PGWRT | PGERS | SPMEN | 180 |
| 0x36 (0x56) | Reserved | – | – | – | – | – | – | – | – | |
| 0x35 (0x55) | MCUCR | JTD | – | – | PUD | – | – | IVSEL | IVCE | 54/69 |
| 0x34 (0x54) | MCUSR | – | – | – | JTRF | WDRF | BODRF | EXTRF | PORF | 43 |
| 0x33 (0x53) | SMCR | – | – | – | – | SM2 | SM1 | SM0 | SE | 33 |
| 0x32 (0x52) | Reserved | – | – | – | – | – | – | – | – | |
| 0x31 (0x51) | OCDR | | | | On-Chip Debug Register | | | | | 174 |
| 0x30 (0x50) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2F (0x4F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2E (0x4E) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2D (0x4D) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2C (0x4C) | Reserved | – | – | – | – | – | – | – | – | |
| 0x2B (0x4B) | GPIOR2 | | | | General Purpose I/O Register 2 | | | | | 25 |
| 0x2A (0x4A) | GPIOR1 | | | | General Purpose I/O Register 1 | | | | | 25 |
| 0x29 (0x49) | Reserved | – | – | – | – | – | – | – | – | |
| 0x28 (0x48) | OCR0B | | | | Timer/Counter0 Output Compare Register B | | | | | 94 |
| 0x27 (0x47) | OCR0A | | | | Timer/Counter0 Output Compare Register A | | | | | 94 |
| 0x26 (0x46) | TCNT0 | | | | Timer/Counter0 (8 Bit) | | | | | 94 |
| 0x25 (0x45) | TCCR0B | FOC0A | FOC0B | – | – | WGM02 | CS02 | CS01 | CS00 | 93 |
| 0x24 (0x44) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | – | – | WGM01 | WGM00 | 90 |
| 0x23 (0x43) | GTCCR | TSM | – | – | – | – | – | PSRASY | PSRSYNC | 106 |
| 0x22 (0x42) | EEARH | – | – | – | – | – | – | – | High Byte | 20 |
| 0x21 (0x41) | EEARL | | | | EEPROM Address Register Low Byte | | | | | 20 |
| 0x20 (0x40) | EEDR | | | | EEPROM Data Register | | | | | 20 |
| 0x1F (0x3F) | EECR | – | – | EEPM1 | EEPM0 | EERIE | EEMPE | EEPE | EERE | 20 |
| 0x1E (0x3E) | GPIOR0 | | | | General Purpose I/O Register 0 | | | | | 25 |
| 0x1D (0x3D) | EIMSK | – | – | – | – | INT3 | INT2 | INT1 | INT0 | 58 |
| 0x1C (0x3C) | EIFR | – | – | – | – | INTF3 | INTF2 | INTF1 | INTF0 | 58 |

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x1B (0x3B) | PCIFR | – | – | – | – | – | – | PCIF1 | PCIF0 | |
| 0x1A (0x3A) | Reserved | – | – | – | – | – | – | – | – | |
| 0x19 (0x39) | Reserved | – | – | – | – | – | – | – | – | |
| 0x18 (0x38) | Reserved | – | – | – | – | – | – | – | – | |
| 0x17 (0x37) | Reserved | – | – | – | – | – | – | – | – | |
| 0x16 (0x36) | TIFR1 | – | – | – | – | – | – | OCF1A | TOV1 | 104 |
| 0x15 (0x35) | TIFR0 | – | – | – | – | – | OCF0B | OCF0A | TOV0 | 95 |
| 0x14 (0x34) | Reserved | – | – | – | – | – | – | – | – | |
| 0x13 (0x33) | Reserved | – | – | – | – | – | – | – | – | |
| 0x12 (0x32) | Reserved | – | – | – | – | – | – | – | – | |
| 0x11 (0x31) | Reserved | – | – | – | – | – | – | – | – | |
| 0x10 (0x30) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0F (0x2F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0E (0x2E) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0D (0x2D) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0C (0x2C) | Reserved | – | – | – | – | – | – | – | – | |
| 0x0B (0x2B) | PORTD | – | – | – | – | – | – | PORTD1 | PORTD0 | 75 |
| 0x0A (0x2A) | DDRD | – | – | – | – | – | – | DDD1 | DDD0 | 75 |
| 0x09 (0x29) | PIND | – | – | – | – | – | – | PIND1 | PIND0 | 75 |
| 0x08 (0x28) | PORTC | – | – | – | – | – | – | – | PORTC0 | 78 |
| 0x07 (0x27) | Reserved | – | – | – | – | – | – | – | – | |
| 0x06 (0x26) | Reserved | – | – | – | – | – | – | – | – | |
| 0x05 (0x25) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 74 |
| 0x04 (0x24) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 74 |
| 0x03 (0x23) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 75 |
| 0x02 (0x22) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTB3 | PORTA2 | PORTA1 | PORTA0 | 74 |
| 0x01 (0x21) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | 74 |
| 0x00 (0x20) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | 74 |

Notes:  1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses $00 - $3F must be used. When addressing I/O registers as data space using LD and ST instructions, $20 must be added to these addresses. The ATmega406 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from $60 - $FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

# 5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **ARITHMETIC AND LOGIC INSTRUCTIONS** | | | | | |
| ADD | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One's Complement | Rd ← 0xFF – Rd | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | Rd ← 0x00 – Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |
| MUL | Rd, Rr | Multiply Unsigned | R1:R0 ← Rd x Rr | Z,C | 2 |
| MULS | Rd, Rr | Multiply Signed | R1:R0 ← Rd x Rr | Z,C | 2 |
| MULSU | Rd, Rr | Multiply Signed with Unsigned | R1:R0 ← Rd x Rr | Z,C | 2 |
| FMUL | Rd, Rr | Fractional Multiply Unsigned | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| FMULS | Rd, Rr | Fractional Multiply Signed | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| FMULSU | Rd, Rr | Fractional Multiply Signed with Unsigned | R1:R0 ← (Rd x Rr) << 1 | Z,C | 2 |
| **BRANCH INSTRUCTIONS** | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| JMP | k | Direct Jump | PC ← k | None | 3 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| CALL | k | Direct Subroutine Call | PC ← k | None | 4 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |
| **BIT AND BIT-TEST INSTRUCTIONS** | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| **DATA TRANSFER INSTRUCTIONS** | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LDD | Rd,Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| STD | Y+q,Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| SPM | | Store Program Memory | (Z) ← R1:R0 | None | - |
| IN | Rd, P | In Port | Rd ← P | None | 1 |

## 5. Instruction Set Summary (Continued)

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| OUT | P, Rr | Out Port | P ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| **MCU CONTROL INSTRUCTIONS** | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## 6. Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package[1] | Operation Range |
|---|---|---|---|---|
| 1 | 4.0 - 25V | ATmega406-1AAU[2] | 48AA | Industrial (-30°C to 85°C) |

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

| Package Type | |
|---|---|
| 48AA | 48-lead, 7 x 7 x 1.44 mm body, 0.5 mm lead pitch, Low Profile Plastic Quad Flat Package (LQFP) |

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# 7. Packaging Information

## 7.1 48AA



Notes: 1. This package conforms to JEDEC reference MS-026, Variation BBC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.
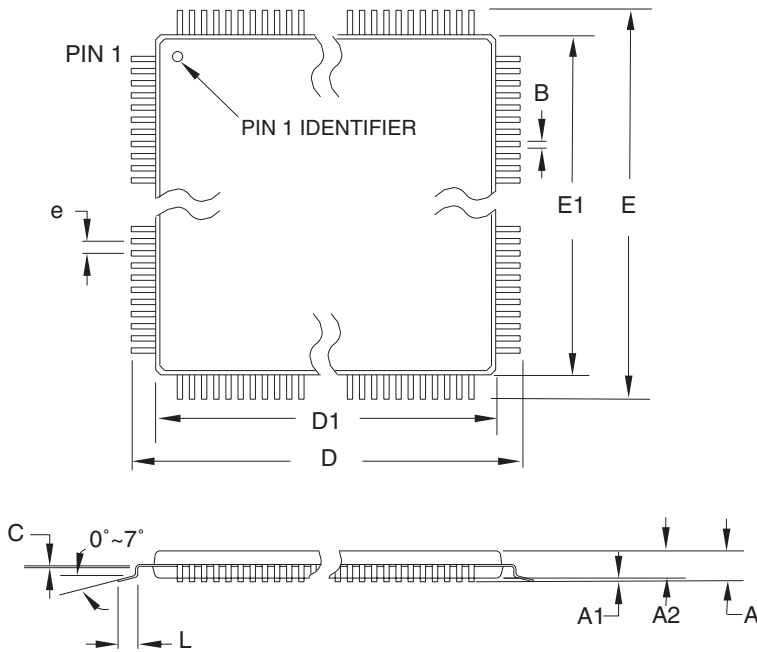
**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------|----------|------|--------|
| A | – | – | 1.60 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 1.35 | 1.40 | 1.45 | |
| D | 8.75 | 9.00 | 9.25 | |
| D1 | 6.90 | 7.00 | 7.10 | Note 2 |
| E | 8.75 | 9.00 | 9.25 | |
| E1 | 6.90 | 7.00 | 7.10 | Note 2 |
| B | 0.17 | – | 0.27 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.50 TYP | | | |

10/5/2001

| 2325 Orchard Parkway San Jose, CA 95131 | **TITLE** **48AA,** 48-lead, 7 x 7 mm Body Size, 1.4 mm Body Thickness, 0.5 mm Lead Pitch, Low Profile Plastic Quad Flat Package (LQFP) | **DRAWING NO.** 48AA | **REV.** C |
|---|---|---|---|

## 8. Errata

### 8.1 All rev.

No known errata.

# 9. Datasheet Revision History

## 9.1 Rev 2548A - 01/05

1. Initial revision.

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